IN THE CLAIMS

Please find below a listing of all of the pending claims. The status of each claim is set forth in parentheses. This listing will replace all prior versions, and listings, of claims in the present application.

1. (Currently amended) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate by,

depositing a layer of material onto the substrate;

imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device,

wherein the semiconductor device comprises a cross-point memory array.

2. (Canceled).

3. (Canceled).

4. (Previously Presented) The method of claim 1 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

5. (Previously Presented) The method of claim 1 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a 3D stamping tool to create the 3D pattern.

6. (Previously Presented) The method of claim 1 wherein imprinting a 3D pattern into the layer of material further comprises utilizing a molding process to imprint the 3D pattern into the layer of material.

7. (Previously Presented) The method of claim 1 wherein the layer of material comprises a polymer material.

8. (Previously Presented) The method of claim 1 wherein the layer of material comprises a photo-resist material.

9. (Previously Presented) The method of claim 1 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

10. (Currently amended) The method of claim [[3]]1 wherein depositing at least one material over the substrate further comprises:

depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

11. (Withdrawn) The method of claim 9 wherein depositing at least one material over the substrate further comprises:

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and

removing the first planarizing polymer.

12. (Withdrawn) The method of claim 11 wherein depositing at least one material over the substrate further comprises:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

13. (Currently amended) A system for forming a semiconductor device comprising:

means for forming a pattern in a substrate wherein the pattern is 3-dimensional, wherein the means for forming the pattern further comprises:

means for depositing a layer of material onto the substrate;

means for imprinting a 3D pattern onto the layer of material; and

means for transferring the 3D pattern into the substrate; and

means for depositing at least one semiconductor material over the substrate in accordance with desired characteristics of the semiconductor device,

wherein the semiconductor device comprises a cross-point memory array.

14. (Canceled).

15. (Canceled).

16. (Currently amended) The system of claim [[14]]13 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

17. (Currently amended) The system of claim [[14]]13 wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

18. (Currently amended) The system of claim [[14]]13 wherein the means for imprinting a 3D pattern into the layer of material further comprises means .for implementing a molding process to imprint the 3D pattern into the layer of material.

19. (Currently amended) The system of claim [[14]]13 wherein the means for transferring the 3D pattern into the substrate includes:

means for removing a portion of the layer of material thereby exposing a portion of the substrate;

means for etching the exposed portion of the substrate;

means for removing another portion of the layer of material thereby exposing a second portion of the substrate;

means for etching the second portion of the substrate; and

means for removing a remaining portion of the layer of material.

20. (Currently amended) The system of claim [[14]]13 wherein the means for imprinting a 3D pattern onto the layer of material further comprises means for utilizing a 3D stamping tool to create the 3D pattern.

21. (Withdrawn-currently amended) The system of claim [[15]]13 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a first metal layer;

means for applying a planarizing polymer to the first metal layer;

means for removing a portion of the planarizing polymer;

means for utilizing the planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

means for etching the substrate in a selective fashion; and

means for removing the planarizing polymer.

22. (Currently amended) The system of claim [[15]]13 wherein the layer of material comprises a polymer material.

23. (Currently amended) The system of claim [[15]]13 wherein the layer of material comprises a photo-resist material.

24. (Withdrawn) The system of claim 21 wherein the means for depositing at least one semiconductor material over the substrate further comprises:

means for depositing a second metal layer on the remaining portion of the first metal layer;

means for applying a second planarizing polymer to the second metal layer;

means for removing a portion of the second planarizing polymer;

means for utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

means for removing the second planarizing polymer.

25. (Withdrawn) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate by,

depositing a layer of material onto the substrate;

imprinting a 3D pattern into the layer of material; and

transferring the 3D pattern into the substrate;

depositing a first metal layer on the substrate;

applying a first planarizing polymer to the metal layer;

removing a portion of the first planarizing polymer;

utilizing the first planarizing polymer as an etch mask to etch the first metal layer thereby leaving a remaining portion of the first metal layer;

etching the substrate in a selective fashion; and

removing the first planarizing polymer.

26. (Withdrawn) The method of claim 25 wherein the semiconductor device comprises a cross-point memory array.

27. (Withdrawn) The method of claim 25 further comprising:

depositing a second metal layer on the remaining portion of the first metal layer;

applying a second planarizing polymer to the second metal layer;

removing a portion of the second planarizing polymer;

utilizing the second planarizing polymer as an etch mask to etch the second metal layer; and

removing the second planarizing polymer.

28. (Canceled).

29. (Canceled).

30. (Withdrawn) The semiconductor device of claim 25 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

31. (New) A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate by,

depositing a layer of material onto the substrate, wherein the substrate comprises a polyimide material;

imprinting a 3D pattern into the layer of material without imprinting the 3D pattern into the substrate; and

transferring the 3D pattern into the substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

32. (New) The method of claim 31 wherein the semiconductor device comprises a cross-point memory array.

33. (New) The method of claim 31 wherein imprinting a 3D pattern into the layer of material further comprises utilizing one of a 3D stamping tool to create the 3D pattern and a molding process to imprint the 3D pattern into the layer of material.

34. (New) The method of claim 31 wherein transferring the 3D pattern into the substrate includes:

removing a portion of the layer of material thereby exposing a portion of the substrate;

etching the exposed portion of the substrate;

removing another portion of the layer of material thereby exposing a second portion of the substrate;

etching the second portion of the substrate; and

removing a remaining portion of the layer of material.

35. (New) The method of claim 31 wherein depositing at least one material over the substrate further comprises:

depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.